

# Physico-chemical and Electrical Characterization of Gate Stacks on GaAs and (In,Ga)As

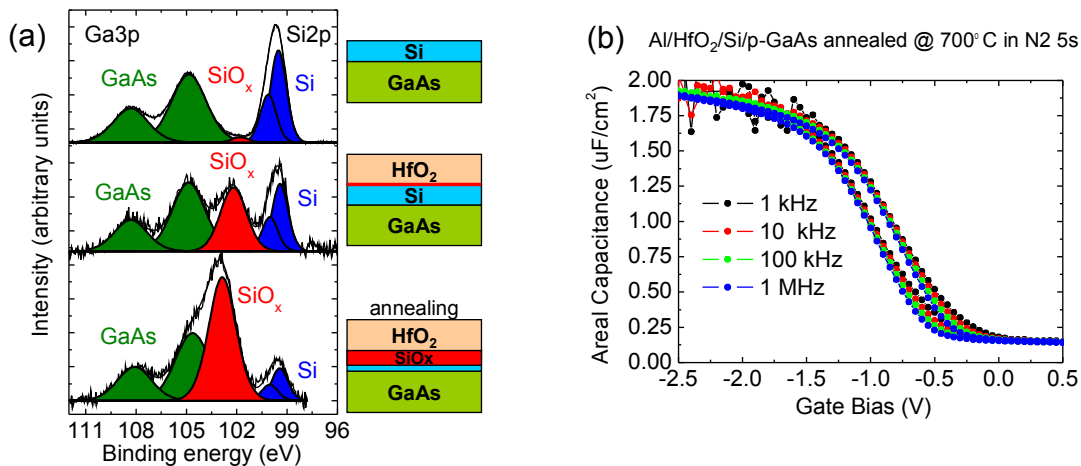
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Due to their higher carrier injection velocity, III-V compound semiconductors are being studied as potential candidates to replace Si as active channel material in C-MOS technology. However, the integration of a suitable gate stack on III-V channels may be even more challenging than the integration of high-k-based gate stacks on Si. The following issues must be addressed: I) efficient cleaning methods leading to clean, stoichiometric and ordered III-V surfaces have to be developed; II) efficient passivating methods to minimize the amount of electrically active defects at the III-V/dielectric interface need to be defined; III) the gate stack must be thermodynamically stable against the temperatures used for gate stack deposition and post-deposition processing like source/drain formation. In particular, substrate oxidation has to be *totally* avoided; IV) gate stack composition must be optimized to achieve high gate capacitance and low defect density in the dielectrics and at their interfaces.

*In-situ* X-ray photoelectron spectroscopy (XPS) is a powerful characterization tool which allows one to address all these issues, providing an excellent feedback for the adjustment of the growth parameters and the post-deposition thermal treatments. This will be shown by discussing the case of GaAs and  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  channels cleaned by remote RF H-plasma in UHV and passivated by a thin layer of amorphous Si before deposition of the high-k oxides [1]. XPS gives a comprehensive picture of the gate stack, ranging from the properties of the cleaned surface (removal of contaminants, stoichiometry, band bending, Fermi level (FL) pinning), to the effect of the passivating layer on the III-V surface (interfacial chemistry, thickness of the passivating layer, valence band offset, FL de-pinning) and to the interaction between the different layers [Figure 1(a)]. Electrical properties of gate stacks on GaAs and  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  channels [Figure 1(b)] will be presented and correlated to the gate stack properties determined by XPS. Finally, we will show how XPS analysis is decisive in determining a gate stack deposition procedure which leads to *scaled* devices with outstanding electrical characteristics.

**Key words :** III-V CMOS, Passivation, XPS



**FIGURE 1.** (a) XPS spectra showing the evolution of the Si passivating layer upon  $\text{HfO}_2$  deposition and post-deposition anneal at 700°C in  $\text{N}_2$  for 5s. (b) Capacitance vs voltage characteristic for an  $\text{Al}/\text{HfO}_2/\text{Si}/\text{p-GaAs}$  MOS capacitor.

1. C. Marchiori, D. J. Webb, C. Rossel, M. Richter, M. Sousa, C. Gerl, R. Germann, C. Andersson, and J. Fompeyrine, *J. Appl. Phys.* **106**, 114 (2009).